REMARKS

In the Office Action dated December 9, 2003, claims 1, 4-9, 23-25, 30-32, and 44 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 6,076,139 (Welker) in view of U.S. Patent No. 6,026,464 (Cohen); and claims 10-22, 26, 28, 33, and 40-41 were rejected under § 103 over Welker in view of Cohen and further view of Xanthaki, "A Memory Controller for Access Interleaving Over a Single Rambus" (Xanthaki).

Applicant acknowledges the indication that claims 27, 29, 34-39, 42, and 43 would be allowable if rewritten in independent form.

As discussed in Applicant's prior Reply to Office Action, claim 1 is not taught or suggested by the asserted combination of Welker and Cohen. There simply is no motivation or suggestion to combine the teachings of Welker and Cohen, as Welker does not disclose plural memory controllers on *a* memory bus. Welker discloses only one memory controller (MIC 310 shown in Figure 3 of Welker) provided on each Rambus channel. Therefore, there is absolutely no *need* in Welker for a priority scheme that defines time slots for access to *a* memory bus.

In response to Applicant's arguments in this regard, the present Office Action cited to Xanthaki for the proposition that it was known to perform access interleaving over a single Rambus. 12/9/03 Office Action at 2-3. Applicant submits that Xanthaki does not provide any teachings that would provide the requisite suggestion or motivation to modify the teachings of Welker to achieve the claimed invention. Note that Xanthaki is also concerned with *one memory controller* on *one* Rambus channel, which is connected to multiple slaves (*see* Figure 2.2 in Section 2.1 of Xanthaki). The access interleaving discussed in Xanthaki refers to interleaving access requests from *one* memory controller or master on the Rambus channel, not from *plural* memory controllers on the Rambus channel. A priority scheme to define access to a memory bus by *plural memory controllers* as recited in claim 1 is quite different from an access interleaving arrangement for requests by only *one* controller, as taught by Xanthaki. Therefore, there is no suggestion by Xanthaki of a priority scheme for defining access by multiple memory controllers on *a* memory bus.

The Office Action then proceeded to cite to passages in columns 5, 7, and 8 of Welker as teaching some type of priority scheme. 12/9/03 Office Action at 3-4. The

cited passages refer to the various masters disclosed in Figure 2 (including processor interface 212, MMP 214, CRTC 216, pipes processor 218, and PCI 220). These masters are connected to the memory interface 200 shown in Figure 2 of Welker, which includes the four MICs 310 depicted in Figure 3. Thus, the priority scheme discussed in Welker refers to the granting of access to any particular MIC 310 to the masters 300, 302, 304, 306, and 308. This does not change the fact that there is still *only one* memory controller on each Rambus channel 202, 204, 206, or 208, as disclosed by Welker. Therefore, because Welker teaches only MIC 310 on one Rambus channel, there is absolutely no motivation to include a priority scheme defining time slots to define access for plural memory controllers onto any of the Rambus channels 202, 204, 206, and 208. Any access interleaving performed on any of the Rambus channels 202, 204, 206, and 208 are performed for requests from only *one* MIC. Therefore, the cited passages of Welker also fail to provide the requisite suggestion or motivation to modify Welker to provide a priority scheme for multiple memory controllers on a memory bus.

Because there exists no motivation or suggestion to combine the teachings of Welker and Cohen in the manner proposed by the Office Action, a *prima facie* case of obviousness has not been established with respect to claim 1.

Furthermore, neither Welker nor Cohen teaches or suggests the predetermined priority scheme of claim 1, where *time slots are allocated to respective memory controllers*. As noted above, only one MIC is connected to each Rambus channel in Welker--therefore, no predetermined priority scheme is disclosed or suggested by Welker for access by plural memory controllers on a memory bus. On the other hand, Cohen describes a request/grant arbitration scheme, where a memory controller that needs access to a memory bus asserts a request signal, with an arbiter asserting a grant signal to enable the memory controller to access the bus. Such a request/grant arbitration scheme is different from a priority scheme defining time slots allocated to respective memory controllers.

Therefore, even if the teachings of Welker and Cohen can be combined, the hypothetical combination of Welker and Cohen does not teach or suggest the subject matter of claim 1.

For the reasons stated above, a *prima facie* case of obviousness has not been established with respect to claim 1.

Independent claim 23 is similarly allowable over the asserted combination of Welker and Cohen, since the asserted combination does not teach or suggest generating memory requests on a memory bus according to a time slot priority scheme that defines time slots allocated to respective memory controllers.

Independent claim 10 was rejected by the present Office Action as being obvious over Welker, Cohen, and Xanthaki. Claim 10 recites a system having a plurality of memory buses and a hub connected to the plurality of memory buses. A plurality of memory controllers are connected to a first one of the memory buses, with each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions. In addition, claim 10 recites that the memory controllers are able to access a second one the memory buses through the hub.

Contrary to the assertion made in the Office Action (12/9/03 Office Action at 10) the MICs 310 in the memory interface 200 (Figure 3) of Welker do not monitor memory requests generated by another memory controller in performing memory-related actions. Because the Office Action has incorrectly applied Welker to the claims, the obviousness rejection is defective on at least this ground.

Also, the hypothetical combination of Welker, Cohen, and Xanthaki fails to disclose or suggest a hub that is connected to a plurality of memory buses, where memory controllers are able to access a second one of the memory buses through the hub.

In response to Applicant's argument in the prior Office Action that neither Welker nor Cohen discloses or suggests a hub that is connected to a plurality of memory buses, the Office Action cited to Xanthaki as suggesting that the Rambus channel can be expanded by attaching one or more Rambus channels via a transceiver forming an interleave memory system (Section 1.2.2). *Id.* at 4-5.

Applicant notes that the expansion of memory described in Section 1.2.2 of Xanthaki refers to attaching more secondary Rambus channels via a transceiver--in other words, more memory devices are added to the additional Rambus channels. Xanthaki teaches only *one* memory controller on the Rambus channels. Thus, even if the transceiver noted in Section 1.2.2 of Xanthaki can be considered the hub, such a

transceiver does not enable a plurality of memory controllers to access a second one of the memory buses through the transceiver. Therefore, no teaching or suggestion has been provided in any of the cited references in this Office Action of the features of claim 10. A *prima facie* case of obviousness has thus not been established with respect to claim 10.

Independent claim 15 is also allowable over the asserted combination of Welker, Cohen, and Xanthaki. Claim 15 recites a method that includes memory controllers generating requests on memory buses connected by a hub, with each memory controller monitoring memory-related actions on the memory buses by at least another memory controller. The asserted combination of Welker and Cohen does not teach or suggest such features.

In view of the foregoing, all independent clams are allowable over the cited references. Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 50-1673 (9295).

Respectfully submitted,

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